Development of a Design Procedure for Class E Amplifiers

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Abstract. Here, the step-by-step design procedure for a Class E amplifier is presented. An existing Class E amplifier system is described using a systems architecture approach. The design decomposition for the case study is written so that Physical Solutions (PSs; equivalent to Design Parameters) are in terms of component parameters (such as frequency or capacitance). Coupling issues are found to arise given constraints on transistor use. The design decomposition is altered to reflect the case where an amplifier is required to power a specific load. A discussion of transistor failure enables a design procedure to be developed by observing path-dependent coupling. The design procedure is tested through the design of a real amplifier. The designed amplifier is built and its performance measured.

1 Introduction

This paper presents the logic of the development of a step-by-step procedure for the design of Class E power amplifiers.

1.1 Motivation

When designing a radio frequency (RF) power amplifier, it is difficult to choose an appropriate transistor to meet the needs of a given application. However, once a transistor is chosen, one of many approaches to computing component values can be used [1–3].

1.2 Systems Design Use

A systems approach is used to clarify the role of the designer, to determine how to choose a transistor based on transistor failure modes, and to specify the requirements for a set of design equations to compute component values. Axiomatic Design (AD) is used identify the logical difficulties in transistor choice by discussing the mathematical consequences of design coupling and to determine an appropriate step-by-step procedure for designing Class E amplifiers.

In this paper, the AD conventions of [4, 5] are used. Conventions of note include:

- A statement of how a system, subsystem, or component is to function is a Functional Requirement (FR).
- A feature of a design which addresses an FR is a Physical Solution[1] (PS).
- Each PS satisfies an FR while observing the relevant design constraints.

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[1] traditionally referred to as a "Design Parameter" [4].

2 Describe/Understand What Exists

To understand the design of Class E amplifiers, an existing case is described: the PRF-1150 RF generator module. The PRF-1150 is a 1 kW, 13.56 MHz RF source developed in 2002 by Directed Energy, Inc. (DEI) [6].

2.1 Describing the PRF-1150

2.1.1 Description Methodology

The understanding of a *System of Interest*[2] (SOI) can be built in several ways:

- by identifying and describing the systems which interact with the SOI (*the surroundings*)
- by describing the relationships among the systems in the surroundings
- by decomposing the SOI into subsystems and describing the relationships among the subsystems
- by describing any of the above from additional viewpoints

For the purposes of describing an existing system employing a Class E amplifier, the SOI is the PRF-1150 module.

2.1.2 Identifying Surroundings

In the PRF-1150 documentation, DEI states [6],

> "DEI has developed an RF module to demonstrate the capabilities of our DEIC420 RF MOSFET gate driver IC and DE275-102N06X2A 1000V 6A RF MOSFET [Metal Oxide Semiconductor Field Effect Transistor] at ISM [Industrial, Scientific, and Medical] frequencies."

[2] Adapted from IEEE 42010, a systems architecture standard [7].

Here, DEI is viewed as the client. The author of [1] served as the designer of the Class E amplifier used in the PRF-1150 module. The PRF-1150 documentation also includes test data taken by an operator or technician. The designer and operator may well have been the same person, but each is treated as a distinct system in the surroundings.

The client, the designer, and the operator not only interact with the SOI, but interact with each other as well. For example, the designer understands the needs of the client and how the operator is going to use the system. Figure 1 shows the relationships between personnel (surrounding systems) and the SOI.

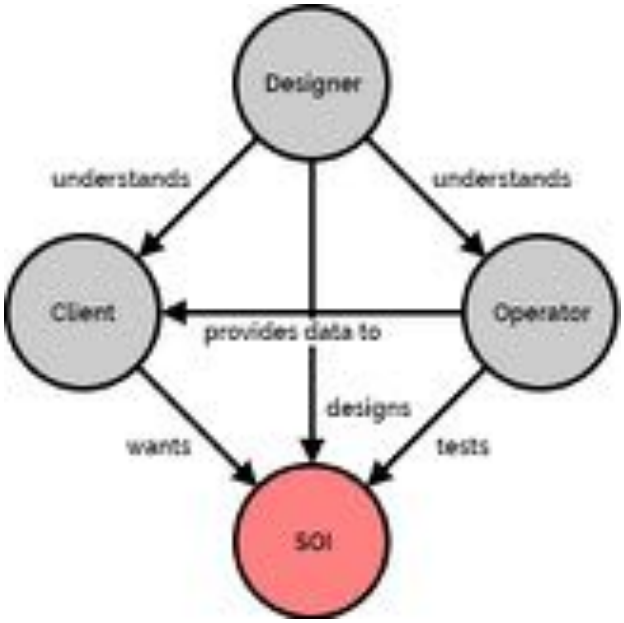

Figure 1. High level relationship diagram for the PRF-1150 and its surroundings. *Understanding relationships in the surroundings of the SOI improves the understanding of the SOI itself.*

2.1.3 Client and SOI

The quote in 2.1.2 describes the client's view of the SOI and can be translated into AD Language:
FR1: Demonstrate the capabilities of the chosen chipset.
PS1: PRF-1150 Module
Constraints:

- $C1a$: The application should be an RF application.
- $C1b$: The operating frequency (f) should be an ISM frequency.
- $C1c$: Use the chosen chipset (MOSFET: DE275-102N06X2A, Gate Driver: DEIC420).

2.1.4 Operator and SOI

A use case can clarify the relationship between the SOI and the operator. Figure 2 shows how the operator and SOI interact with many other systems when the PRF-1150 is being tested. The use case is developed from descriptions in [6].

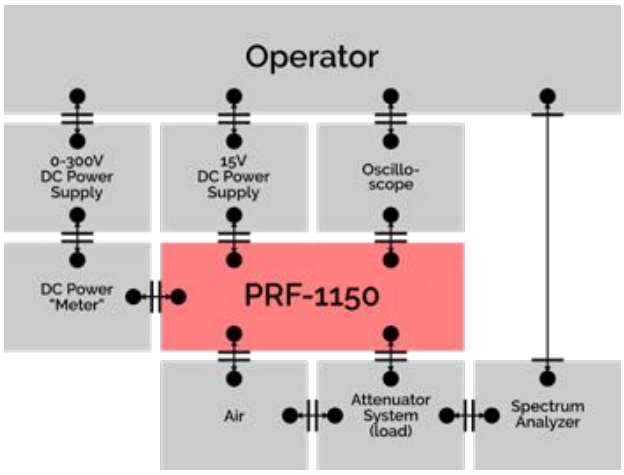

Figure 2. Relationship diagram for the use of the SOI by the Operator. *The operator operates power supplies and takes measurements of the PRF-1150. This is a more specific way to state the original relationship between the SOI and the Operator.*

The operator controls the SOI by turning on or off power supplies and by adjusting the output voltage of the 0-300 V DC source. The 0-300 V DC source provides electrical power to the SOI as measured by the DC power meter. Figure 3 depicts the use case from a physics viewpoint by detailing the energy transfer into and out of the SOI.

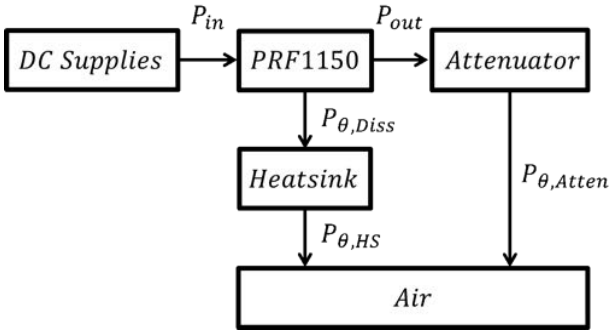

Figure 3. Power distribution diagram of the use case of Figure 5. *Note: these powers are average powers. Also note: the heat sink is included in the PRF-1150 system, but is intentionally called out here to introduce the thermal power dissipated by the SOI.*

Where

- P_{in} = DC power supplied to SOI
- P_{out} = RF output power of SOI
- $P_{\theta,Diss}$ = thermal power dissipated by SOI
- $P_{\theta,HS}$ = thermal power dissipated by the heat sink = $P_{\theta,Diss}$
- $P_{\theta,Atten}$ = thermal power dissipated by attenuator = P_{out}

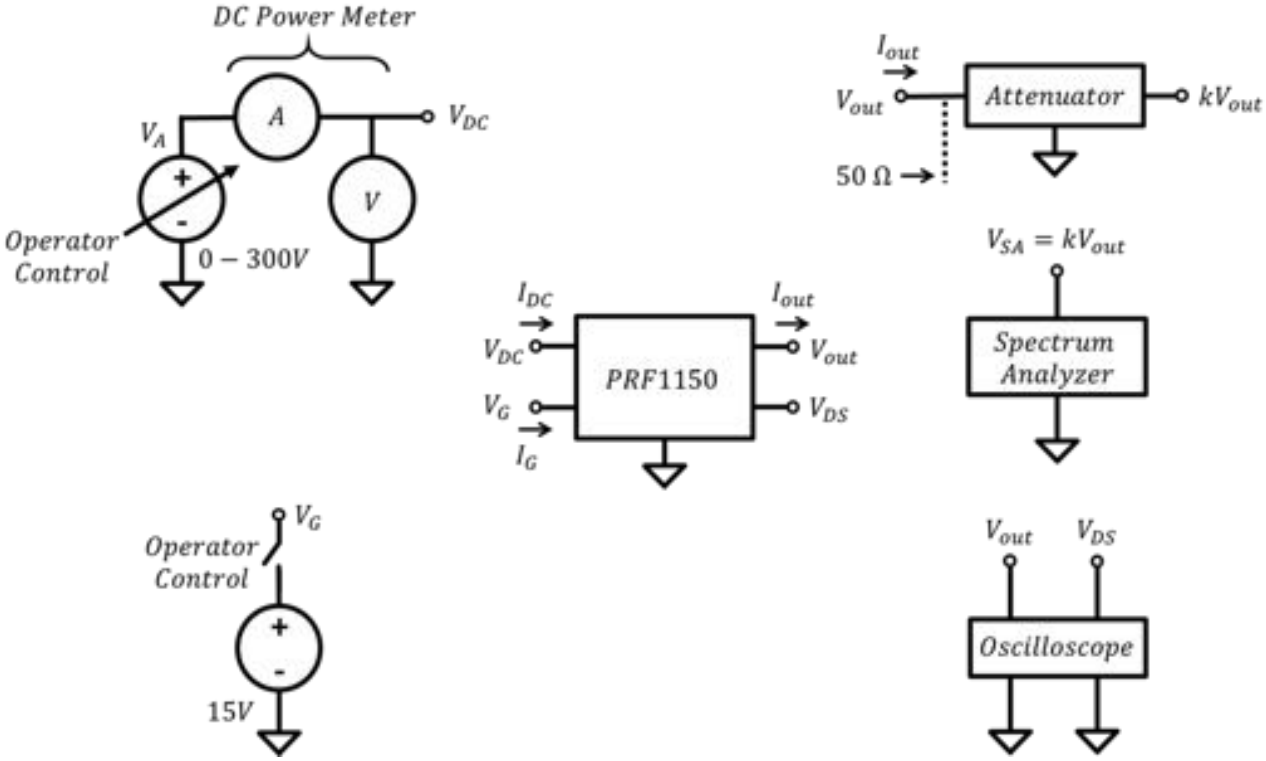

Figure 4. Electrical representation of relationships among surrounding subsystems and SOI.

Figure 4 furthers the energy transfer description of Figure 3 by calling out the voltages and currents among interactors.[3] The voltages and currents are:

- $V_A = V_{DC}$ = main DC supply voltage to the SOI (0 V to 300 V)
- I_{DC} = current supplied to the PRF-1150 via the main DC power supply
- $V_G = 15V$ = secondary DC supply voltage to the SOI
- I_G = current supplied to the PRF-1150 via the secondary DC power supply
- V_{out} = RF output voltage of SOI
- I_{out} = RF output current of the SOI
- $V_{SA} = kV_{out}$ = attenuated V_{out} as measured by the spectrum analyzer
- V_{DS} = an internal voltage of the SOI measured externally[4]

2.1.5 Designer, SOI, and SOI Subsystems

To effectively design the SOI, the designer needs to understand the inner workings of the SOI as well as its surroundings. The schematics and descriptions in [6] are used to construct Figure 5 - a view of the PRF-1150 subsystems.

The signal source output is amplified by the gate driver to provide a switching signal (V_{GS}) for the Class E amplifier. A heat sink aids in the dissipation of thermal power

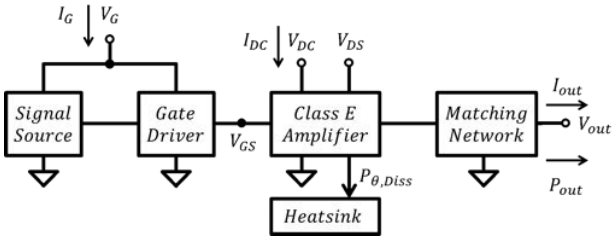

Figure 5. The main electrical subsystems internal to the PRF-1150

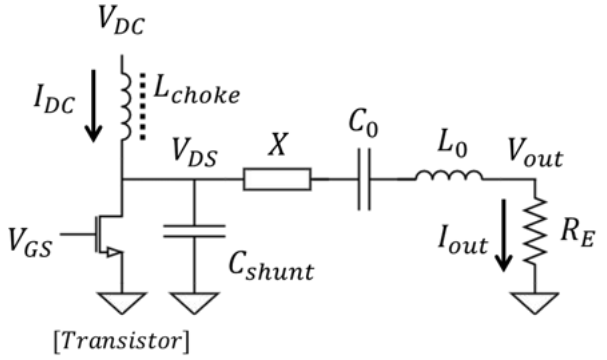

Figure 6. Conventional Class E Circuit

(as in Figure 3). The output impedance of the amplifier is matched to a load via the matching network.

[3] The accuracy of the description is limited by assuming that the measurement currents are negligible from the view of the SOI.

[4] This voltage is described more specifically in 2.1.5

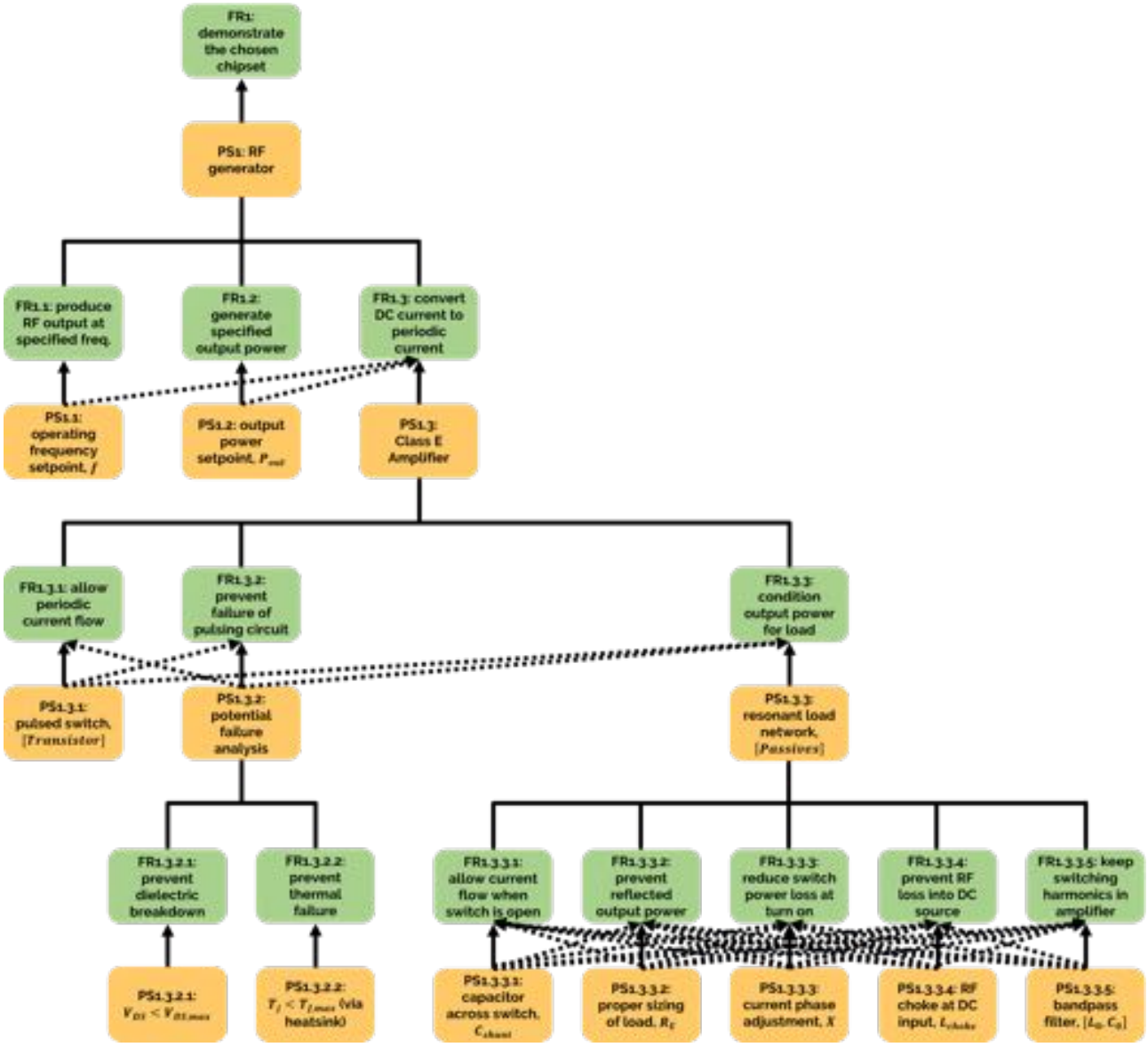

Figure 7. Design Decomposition of a Class E amplifier

Class E Amplifier Subsystem

The Class E arrangement used in the PRF-1150 is as the original arrangement presented by N. Sokal and A. Sokal in 1975 [8]. Figure 6 shows the general Class E amplifier schematic.
Here,

- V_{GS} = the RF input signal to the Class E amplifier
- $[Transistor]$ = a switch controlled by the input signal (typically a MOSFET)[5]
- V_{DS} = voltage across the switch
- L_{choke} = inductance of the RF choke (only allows DC current to flow)
- C_{shunt} = capacitance across switch to allow RF current to flow when switch is open
- $[C_0, L_0]$ = bandpass filter
- R_E = load resistance required for Class E operation
- X = extra reactance in series with the Class E load network R_E, L_0, C_0

2.2 Design Decomposition

Using [1, 3, 9], the Class E portion of the SOI can be described with a design decomposition (Figure 7). The coupling[6] shown here is determined via the equation sets in [1, 3, 9, 10] and by consideration of potential failure modes (discussed in 3.0.1).

[5] A note about notation: $[item]$ = the set of constants and variables specific to *item*. For a car, $[car] = [make, model, year, color, ...]$.

[6] AD, the unintentional relationships (coupling) between PSs and FRs is shown with dashed arrows [5]. Coupling means that the PS of one FR affects the accomplishment of another FR. In some cases, the coupling between two FR-PS sets is only path-dependent (partial). For example, if two FRs (FR_A and FR_B) are accomplished by two PSs (PS_A and PS_B respectively) and PS_A affects the accomplishment of FR_B, then by implementing PS_A before PS_B a recursion can be avoided.

2.2.1 Passive Component Coupling

In the field of electronics, the traditional Class E amplifier is well understood at a component level [1–3, 8, 9]. Since the introduction of the Class E amplifier, papers have been written which relate the operation of the Class E amplifier (output power, frequency, harmonic content) to the values of the passive circuit elements [1–3]. While the specific relationships vary from paper to paper, overall, the variables related are the same. It is possible that more sets of passive component equations will be developed in the future. Therefore, these equations are expressed in a general form (equation 1).

$$[Passives] = E_{passives}([Op], [Transistor], V_{DC}) \quad (1)$$

Where,

- $[Passives] = [X, L_0, C_0, L_{choke}, C_{shunt}, R_E]$ = set of passive component values constituting the resonant load network
- $[Op] = [P_{out}, f]$ = set of operating parameters (output power and frequency)
- $[Transistor]$ = set of relevant characteristics of the chosen transistor
- $E_{passives}$ = set of Class E equations to compute $[Passives]$

As a given set of operating conditions, $[Op]$, results in a single point in the space of $[Passives]$ which will behave as a Class E amplifier [1–3, 8, 9], the complete coupling in the resonant load network branch of the design decomposition (PS 1.3.3) will not be an optimization problem if the path-dependency of the design is followed. Instead, it is a single PS (a complete set of parameters) to a single FR (FR1.3.3).

2.2.2 Transistor-First Design

For the Class E amplifier in the PRF-1150, the designer was constrained to a particular choice of transistor ($C1c$). That is, PS 1.3.1 was implemented first - despite path-dependent coupling suggesting otherwise (PS 1.1 and PS 1.2 before PS 1.3). Figure 8 shows the optimization problem caused by the partial implementation of PS 1.3 before PS 1.1 and PS 1.2. By choosing an operating frequency at this point (13.56 MHz in the case of the PRF-1150), the number of free variables is reduced to one, P_{out}. As $FR1$ is to demonstrate the capabilities of the chipset, maximizing P_{out} would serve this FR well. Maximizing is indeed an optimization problem.

Transistor-First Design Procedure

Currently, the design decomposition and the PRF-1150 description suggest the following procedure:

1. **Choose a transistor**
2. **Choose an operating frequency**
3. **Choose a set of passive equations,** $E_{passives}$

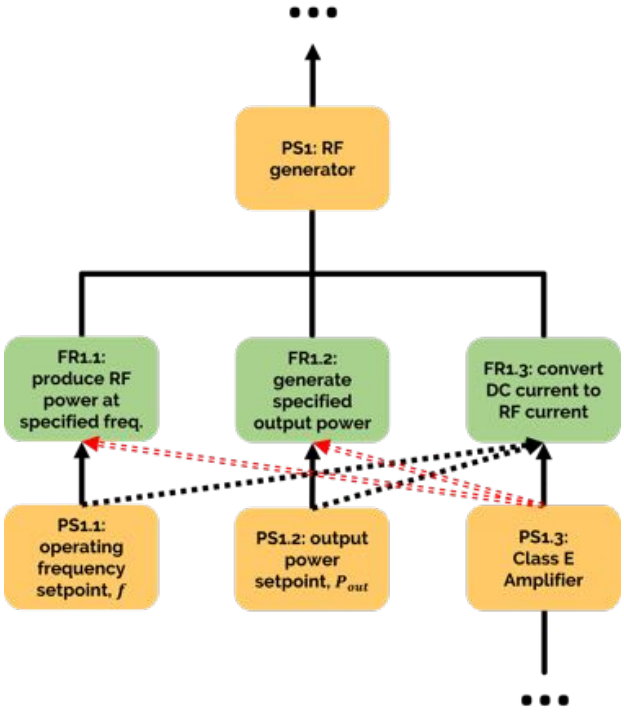

Figure 8. Optimization problem caused by choosing a transistor first. *The red lines show the forced direction of the relationship between PSs and FRs.*

4. **Maximize the output power by manipulating** $[Passives]$**.**[7]

3 Adapt/Improve What Exists

When an amplifier is needed to power a particular load, there is no constraint on transistor use. Instead, the given load requires a specific amount of RF power at a specific frequency - a specific set of operating parameters, [Op]. For example, the authors have determined that a particular plasma experiment requires at least 1 kW of RF power at a frequency of 13.56 MHz. There are no restrictions on transistor use other than keeping costs low. The authors have access to a heat sink with a thermal resistance of 0.1 $°C/W$.

3.0.1 Transistor Failure

To design a Class E amplifier for a given $[Op]$, the maximum power required by the load should coincide with the maximum power output power of the amplifier. To find the maximum output power of the amplifier, it is important to understand what is meant by "maximum"

[7] Choosing the transistor first no longer allows a single point in $[Passives]$ to be computed easily (as per Eq 1). Instead, $E_{passives}$ is used to maximize P_{out} with respect to $[Passives]$.

and what happens when the maximum output power is *exceeded*. Passive components such as inductors and capacitors are of low enough cost that these typically will not be what limit the output power. The transistor, often the most expensive component, is the bottleneck. At an output power just above the maximum, the transistor will fail. A transistor can fail in two ways (which are relevant): dielectric breakdown of the junction or excessive temperature [11].[8] Both of these result in irreparable physical and chemical change to junction itself.

Dielectric Failure

Avoiding dielectric breakdown ($FR1.3.2.1$) is straightforward. A transistor's datasheet [12, 13] provides a maximum voltage rating between the drain and source of the device ($V_{DS,max}$). As the voltage across the device is proportional to the electric field in the junction, exceeding $V_{DS,max}$ guarantees dielectric breakdown. In operation, maintaining $V_{DS} < V_{DS,max}$ at all times ($PS1.3.2.1$) will prevent dielectric failure. As the operation of the amplifier is determined by component choice, $E_{passives}$ must consider the maximum drain-source voltage experienced by the transistor in terms of the rest of the Class E parameters.

Thermal Failure

Preventing thermal failure is not straightforward. The junction temperature is determined by how much thermal power the transistor is dissipating (P_{diss}), the ambient temperature, and the total thermal resistance between the junction and the ambient thermal mass (air, water, etc.). To facilitate thermal power dissipation (reduce the total thermal resistance), the transistor is mounted to a heat sink. The thermal resistance between the junction and the heat sink depends on the transistor, the heat sink, and the quality of the mounting. For a given heat sink and ambient temperature, the maximum allowable power dissipation is [11] (equation 4)

$$P_{diss,Max} = \frac{T_{J,Max} - T_{Ambient}}{(R_{\theta,J-HS} + R_{\theta,HS-Ambient})} \tag{4}$$

Where

- $P_{diss,Max}$ = maximum power dissipated by the transistor
- $T_{J,Max}$ = maximum junction temperature of the transistor
- $T_{Ambient}$ = ambient temperature
- $R_{\theta,J-HS}$ = total thermal resistance between the junction and the heat sink
- $R_{\theta,HS-Ambient}$ = thermal resistance between heat sink and the ambient thermal mass

[8] Note: *excessive current* is not a root cause of failure. A transistor's current rating is derived from its maximum junction temperature and by assuming that it is mounted to an ideal heat sink [12].

Maximum Output Power and Dissipated Power

Maximum output power occurs when the thermal power dissipated by the transistor is also at a maximum (as long as $V_{DS} < V_{DS,max}$). The maximum allowed dissipated power depends on transistor parameters, $[Transistor]$, and heat sink parameters, $[HS]$. A larger heat sink allows a smaller transistor to be used. A larger transistor allows a smaller heat sink to be used. These sets of parameters are coupled. Choosing a transistor first, as in [6], still leaves the output power and the heat sink undetermined. Choosing the output power first (by choosing $[Op]$) still leaves the transistor and heat sink undetermined - another optimization problem (with respect to cost).

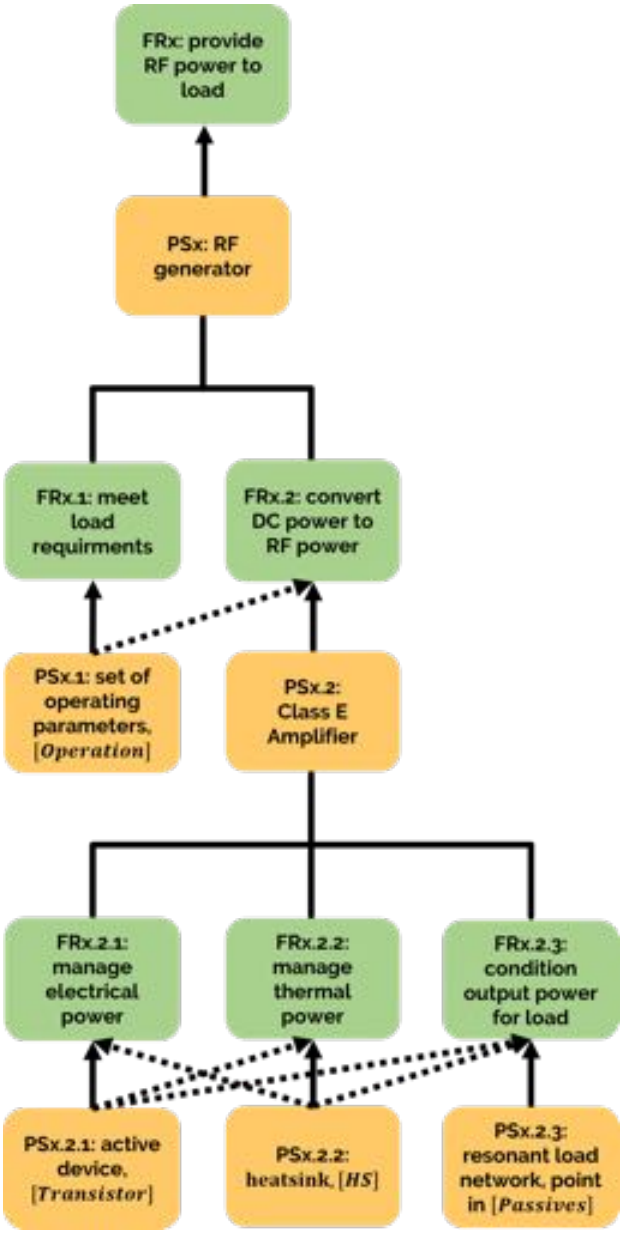

Figure 9. Simplified design decomposition for Application-First Design. *The number x is used to denote that FRx is part of a larger design decomposition*

3.1 Application-First Design

When the application is determined first, $PS\,1.1$ and $PS\,1.2$ can be implemented before $PS\,1.3$. This is consistent with the coupling shown in the design decomposition (Figure 7).

3.1.1 Rearranging the Design Decomposition

Manipulation of the design decomposition will allow further steps to be more obvious. As $FR1.3.1$ and $FR1.3.2$ depend on $[Transistor]$ and $[HS]$, the PSs related to $FR1.3.1$ and $FR1.3.2$ should be the physical components, transistor and heat sink. This requires the rewriting of $FR1.3.1$ and $FR1.3.2$. The rewritten FRs should contain the same information as the original FRs. The resulting design decomposition is shown in Figure 9.

3.1.2 Application-First Design Procedure

Coupling in the updated design decomposition prescribes the following procedure for designing Class E amplifiers.

1. **Identify the RF power and frequency for the application, $[Op]$.**
2. **Choose an appropriate set of design equations.**[9]
3. **Simultaneously choose a transistor and a heat sink.**
4. **Compute the passive component values.**

Step 3 is not practical as it requires an ideal relationship which describes the coupling in the lowest level of the updated design decomposition:

$$([Transistor], [HS]) = F([Op]) \tag{2}$$

Where F is a function which, given a set of operating parameters, outputs all of the needed PSs for the corresponding Class E amplifier. This is not possible, but a tool may be developed to allow it to be accomplished. By using the maximum output power optimization technique in section 3.0.1, the maximum output power, $P_{out,max}$, of a transistor-heat sink combination can be computed for any frequency. The region bounded by $P_{out,max}(f)$ (and the $P_{out,max}$ and f axes) forms the allowed region of $[Op]$ for the chosen transistor and heat sink. If the allowed operating region (Transistor Capability) is computed for every possible combination of transistor and heat sink in a library of transistors and heat sinks, then, given $[Op]$, the transistor-heat sink sets which are capable of meeting the operating setpoints can be found. From the remaining sets of transistors and heat sinks the lowest cost option can be chosen.

[9] As discussed in 3.0.1, the design equations must include considerations for P_{diss} and V_{DS}.

4 Proof of Concept

4.1 Library Development

The authors start with a library of 3 transistors and 1 heat sink to demonstrate the design process. The heatsink is part of an author-built amplifier prototyping kit and the 3 transistor candidates were identified via their application notes:

- Transistor 1: DE275X2-102N06A MOSFET [6]; $69.26 (Newark, 7 May 2018)
- Transistor 2: IXZ631DF12N100 MOSFET and driver [12]; $64.09 (Mouser, 7 May 2018)
- Transistor 3: DFR1200 MOSFET and driver [13]; $145.62 (Mouser, 7 May 2018)

For each of the transistor-heat sink combinations, the operating region is computed (using the Class E equations in [1, 10]) (Figure 10).

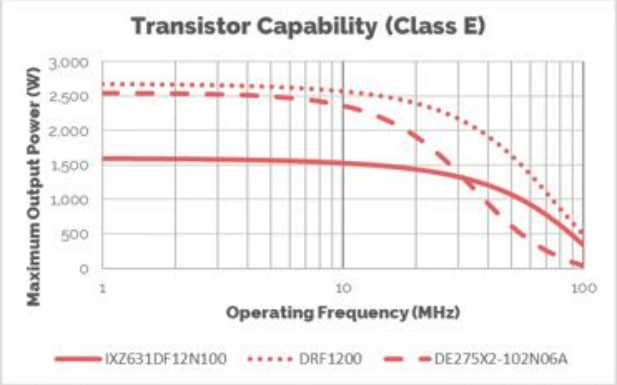

Figure 10. Operation Capability of Transistor-Heat Sink Combinations

4.2 Application-First Design of a Class E Amplifier

1. **Identify the RF power and frequency for the application.**

   $$[Op] = [P_{out}, f] = [1\ kW, 13.56\ MHz]$$

2. **Choose an appropriate set of design equations.**

   The chosen design equations are from [1, 10].

3. **Simultaneously choose a transistor and a heat sink.**

   As all three of the transistor-heat sink combinations in the library are capable of meeting the operating requirements, the combination with the lowest cost and fewest number of consequences (read as "lowest information content") is chosen, Transistor 2 and Heat Sink 1 (the only heat sink in the library).

4. **Compute the passive component values.** Using the chosen design equations, the passive values and supply voltage are computed to be:

   - $X = 24.97\ \Omega$
   - $L_0 = 57.45\ nH$
   - $C_0 = 2.4\ nF$
   - $L_{choke} = 20\ \mu H$
   - $C_{shunt} = 177\ pF$
   - $R_E = 14.93\ \Omega$
   - $V_{DC} = 260\ V$

4.3 Implementation

The design was simulated using LTspice and found to meet the given operating requirements. A prototyping kit was used to quickly implement the design. As is standard [6, 14], an L-type matching network was added to the output of the Class E amplifier to match the output impedance (R_E) to 50 Ω. The resulting amplifier is shown in Figure 12.

The amplifier was tested as in the use case of Figure 2. An exception being that the attenuator was replaced by an author-built, 50 Ω test load (called out in Figure 11). The voltage across this load was measured via a 200 MHz, 100:1 oscilloscope probe (BK Precision PR200B) and a 200 MHz oscilloscope (Siglent SDS 1202CNL+). The time-resolved voltage and calibration data taken for the load-probe system (reflection coefficient measured via Rohde & Schwarz ZVA 24) were used to compute the output power of the amplifier with respect to frequency via Matlab. The measurement setup is shown in Figure 11.

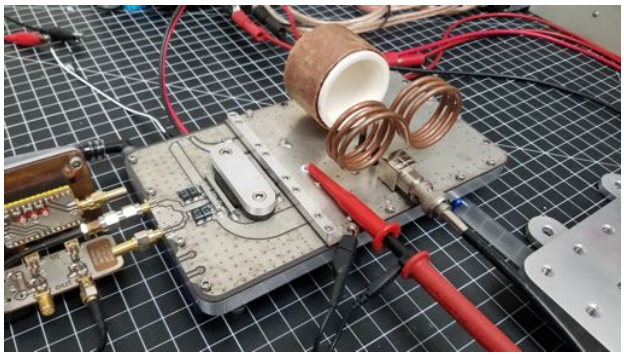

Figure 12. The designed amplifier is implemented with the prototyping kit.

4.4 Measurement Data

The maximum output power measured was 866 W (input power: 1163 W). Higher powers than this would exceed the maximum output power of the DC power supply used (48 V to 280 V, 1200 W). Figure 13 shows the efficiency of the amplifier with respect to the output power.

At an output power of 866 W, the spectral content is as shown in Figure 14. The spectrum is normalized with respect to the output power at the fundamental frequency (13.56 MHz). The second harmonic (27.12 MHz) is 19.07 dB lower than the fundamental. In linear units, the ratio between output powers at the second and first harmonics is 0.012.

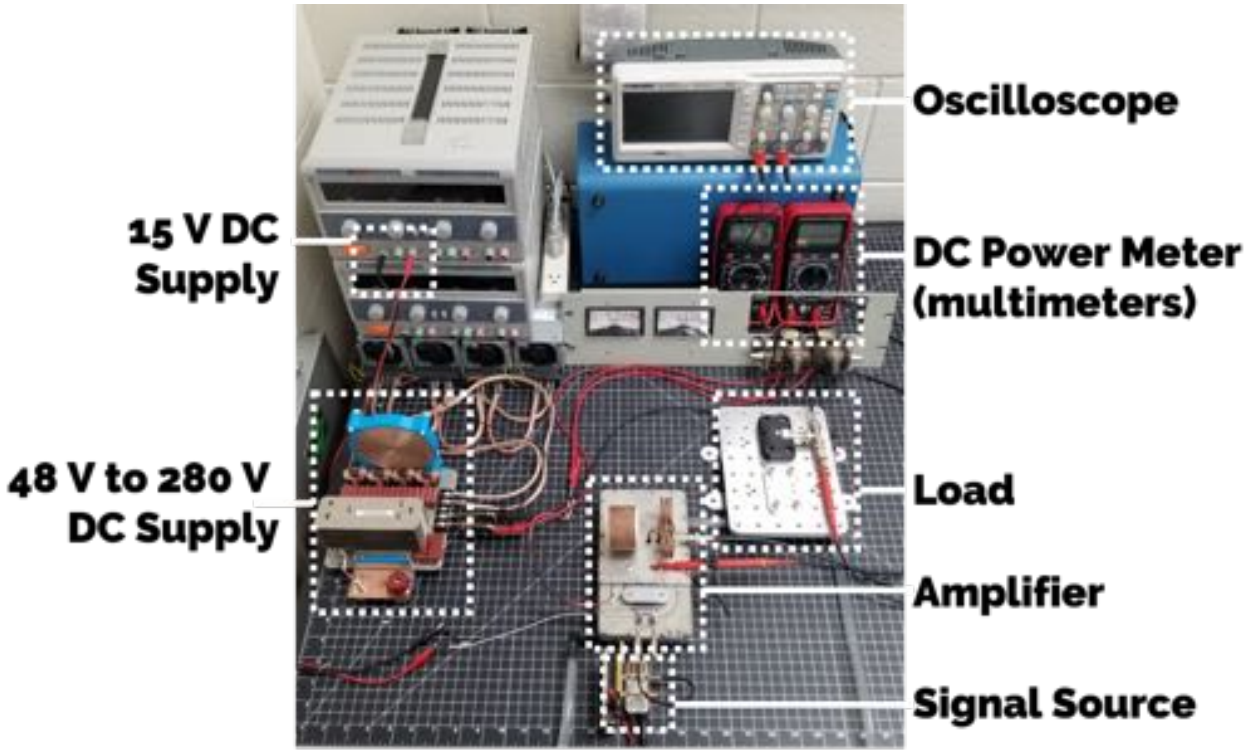

Figure 11. The prototyping kit and its surroundings for charactering the RF output power and DC input power

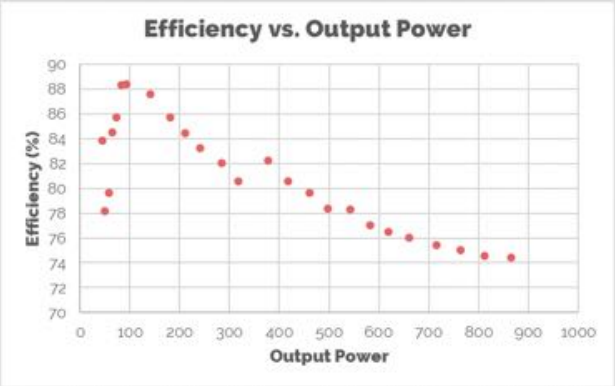

Figure 13. Amplifier Efficiency

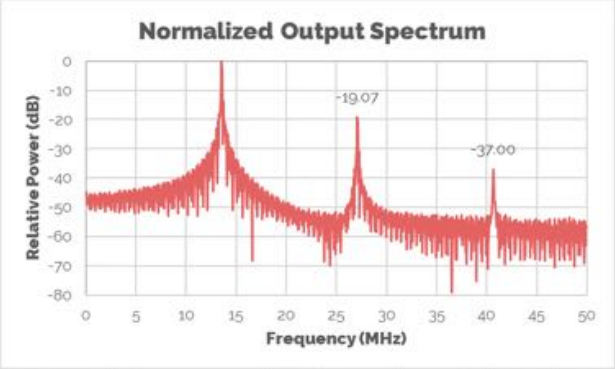

Figure 14. Output spectrum of amplifier up to 3rd harmonic (output power is 866 W)

5 Conclusion

An existing Class E amplifier system was described using a design decomposition. When the design was subjected to the constraint of a client-chosen transistor, coupling issues arose. The resulting optimization of output power was with respect to at least six other PSs. By shifting FR1 to reflect an the Application-First design of a new amplifier and by removing the transistor choice constraint, the remaining optimization problem became manageable by computing the operating range for sets of heat sinks and transistors. An Application-First design procedure was developed and tested using a library of transistor-heat sink pairs.

6 Future Work

6.1 Transistor and Heat Sink Library

The library used in the proof of concept was limited. Future amplifier designs would benefit from a choice among many more options.

6.2 Note about Choosing Specific Components

The design procedure presented here only discusses how to choose passive component values, not specific components. The actual parts can be chosen by way of the second design axiom [4]. The design procedure should be expanded to include the choice of real components.

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